

METHODS FOR FORMING ROUGH RUTHENIUM-CONTAINING

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LAYERS AND STRUCTURES/METHODS USING SAME

This is a divisional of patent Application serial number 09/589,849, filing date 6/8/2000 (PAT NO 6,429,127)

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12/11/03

Field of the Invention

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The present invention relates to semiconductor devices and the fabrication thereof. More particularly, the present invention pertains to rough conductive layers of ruthenium and/or ruthenium oxide.

Background of the Invention

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In the fabrication of integrated circuits, various conductive layers are used. For example, during the formation of semiconductor devices, such as dynamic random access memories (DRAMs), conductive materials are used in the formation of storage cell capacitors and also may be used in interconnection structures, e.g., conductive layers of contact holes, vias, etc.

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As memory devices become more dense, it is necessary to decrease the size of circuit components forming such devices. One way to retain storage capacity of storage cell capacitors of the memory devices and at the same time decrease the memory device size is to increase the dielectric constant of the dielectric layer of the storage cell capacitor. Therefore, high dielectric constant materials are used in such applications interposed between two electrodes. One or more layers of various conductive materials may be used as the electrode material.

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Further, to increase the capacitance for a storage cell capacitor of a memory device without increasing the occupation area of the storage cell capacitor, various techniques have been used to increase the surface area of the lower electrode of the capacitor. For example, hemispherical grains (HSG) have been used to enhance such surface area of the lower electrode of a capacitor of a memory device.